Crystal Clear Technology

Product Specification

T3224W01B00

Crystal Clear Technology sdn. bhd.
16Jalan TP5—Taman Perindustrian Sime UEP
47600 Subang Jaya—Selangor DE
Malaysia. T: +603 80247099 F: +603 80247098

1.0 Table of contents

2.0 Record of revision

Rev	Date	Item	Page	Comment	Originator	Checked By
1.0	28/02/13			Initial Release	Wai Hong	Azhar
2.0	15/05/14	10.1	21	Initialization code revised	Wai Hong	Azhar

3.0 General specification

Panel size: 3.5 inch

Display format: Graphics 240 (w) x 320 (h) dots

Dot pitch: 0.222 (w) x 0.222 (h) mm

Active area: 53.28 (w) x 71.04 (h) mm

General dimensions: 60.6 (w) x 82.0 (h) x 3.8 (t) mm

Color pixel arrangement: Mono stripe

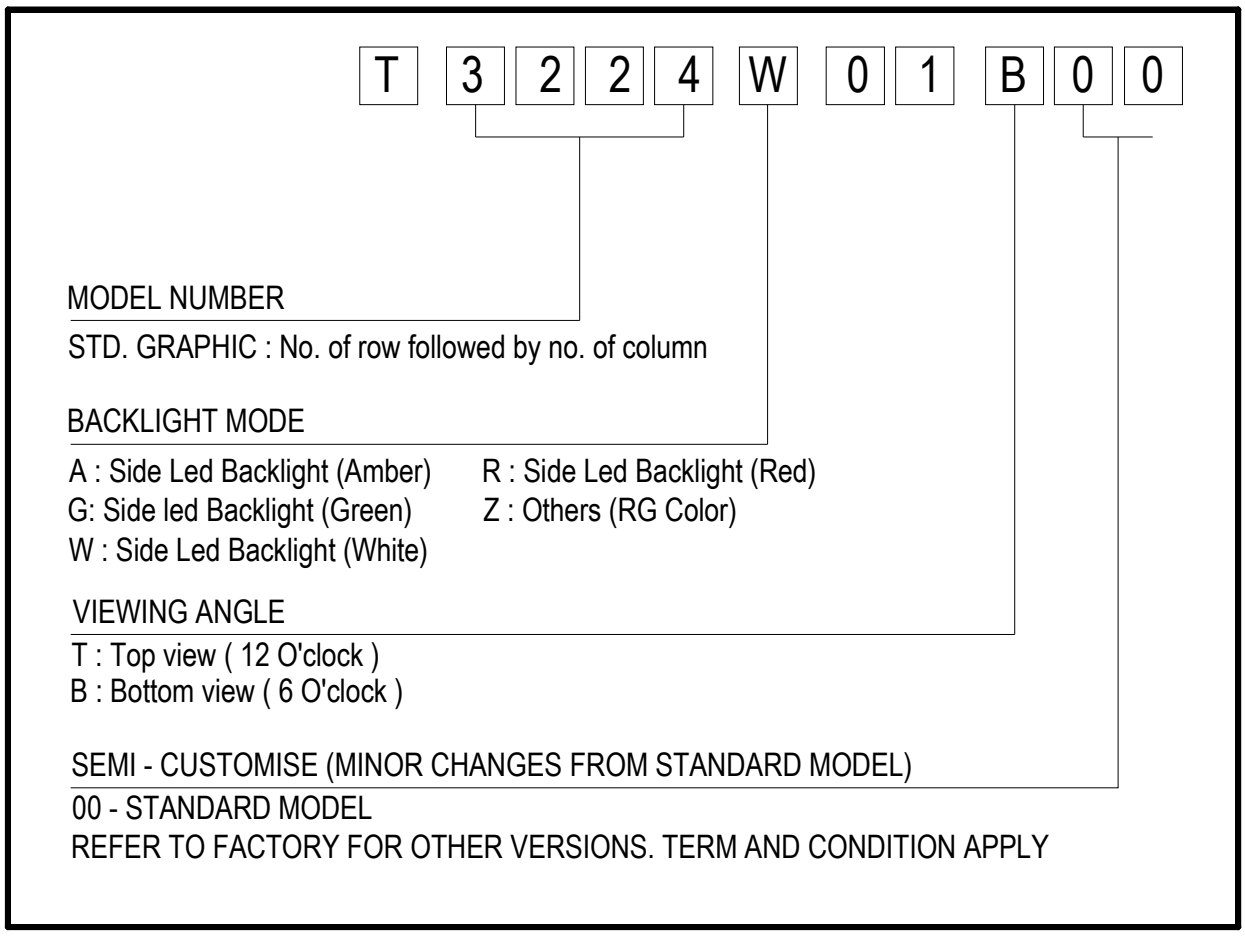
Display mode: Normal Black

Driving method: TFT active matrix

Viewing direction: 6 O'clock

LCD controller / driver: ST7511 or equivalent

Interface: LCD controller / driver – Parallel 6800 / 8080, 4-line serial, 3-line serial



4.0 Absolute maximum rating (at Vss = 0V, ambient temperature = 25°C)

NO	ITEM	SIMBOL	MIN	MAX	UNIT
1.	Power Supply Voltage	VDDI, VDDA	- 0.3	6.0	V
2.	LCD Power Supply Voltage	AVDD, GVDD		7.0	V
		AVCL, GVCL, VCOM		- 7.0	V
		VGH - VGL		35.0	V
3.	MCU Interface Input Voltage	V_{IN}	- 0.3	VDDI+0.3	V
4.	Operating Temperature	T_{op}	-20°C to +70°C		°C
5.	Storage Temperature	T_{st}	-30°C to +80°C		°C

5.0 Electrical characteristics

NO	ITEM	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
1.	Operating Voltage	VDDI, VDDA	-	2.7	-	5.5	V
2.	Operating Voltage	VCCO	Built-in power	-	1.8	-	V
3.	Operating Voltage	AVDDO	Built-in power	6.1	-	9.0	V
4.	Operating Voltage	AVCLO	Built-in power	- 9.0	-	- 6.1	V
5.	Operating Voltage	GVDD	Built-in power	3.1	-	6.2	V
6.	Operating Voltage	GVCL	Built-in power	- 6.2	-	- 3.1	V
7.	Operating Voltage	VGH	Built-in power	8.0	-	19.0	V
8.	Operating Voltage	VGL	Built-in power	- 15.0	-	- 5.0	V
9.	Operating Voltage	VCOM	Built-in power	- 2.0	-	- 0.425	V
10.	“H” Input Voltage	V_{IH}	-	0.8VDDI	-	VDDI	V
11.	“L” Input Voltage	V_{IL}	-	V_{SS}	-	0.2VDDI	V
12.	“H” Output Voltage	V_{OH}	VDDI=2.7V, I_{OL}=1mA	0.8VDDI	-	VDDI	V
13.	“L” Output Voltage	V_{OL}	VDDI=2.7V, I_{OL}=1mA	V_{SS}	-	0.2VDDI	V
15.	Current Supply	I_{DD}	-	-	-	-	A

5.1 Backlight Options

NO	COLOR	FORWARD VOLTAGE (V)			FORWARD CURRENT (mA)			TYPICAL BRIGHTNESS (cd/m2) *
		Min	Typ.	Max	Min	Typ.	Max	
1.	White	-	3.3	-	-	150	200	3000

*Note: 1. Brightness measured at backlight surface.
2. On LCD surface, brightness is only about 10% to 15% of backlight brightness.
3. Lifetime of backlight: For YG, Amber, Red = 20K hrs. For White, Green = 10K hrs

6.0 Environmental requirements

NO	ITEM	CONDITION
1.	Operating Temperature	-20°C to +70°C
2.	Storage Temperature	-30°C to +80°C
3.	Operating Humidity	5% to 95%RH
4.	Cycle Test	0 C @ 30 min to 50 C @ 30min for 1 cycle run for 10 cycles
5.	Lifetime	50000 HOURS (excluding backlight)

*Note: The background color and contrast ratio of LCD will vary throughout operating temperature range.

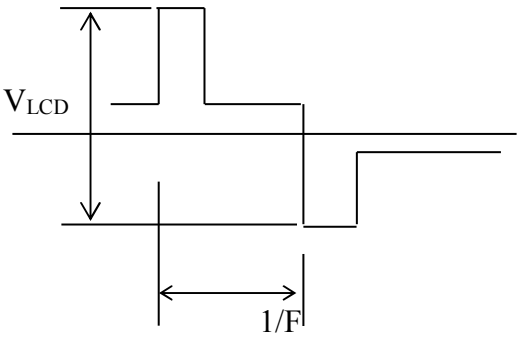
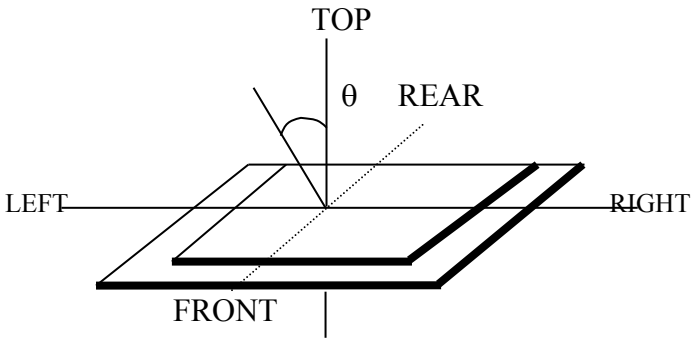
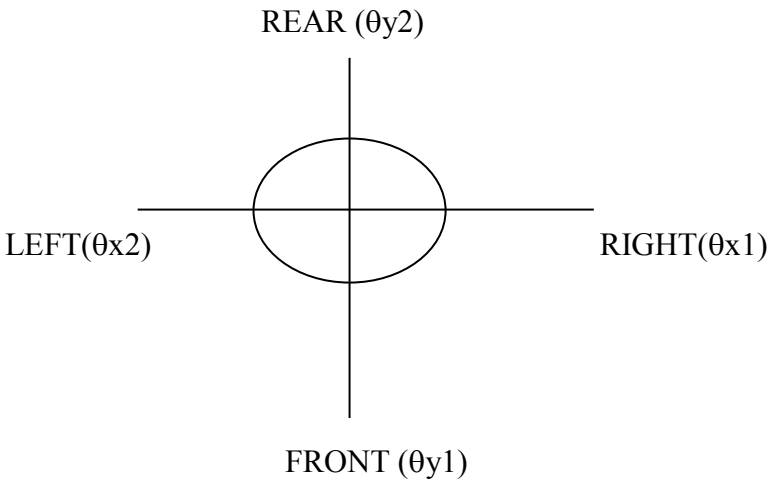
7.0 LCD specification

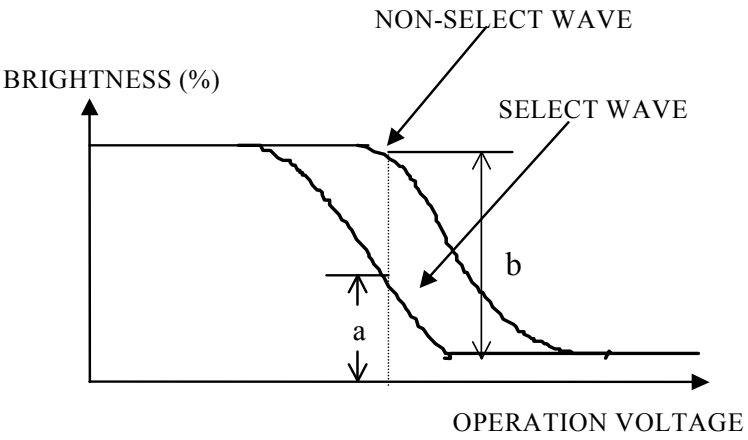
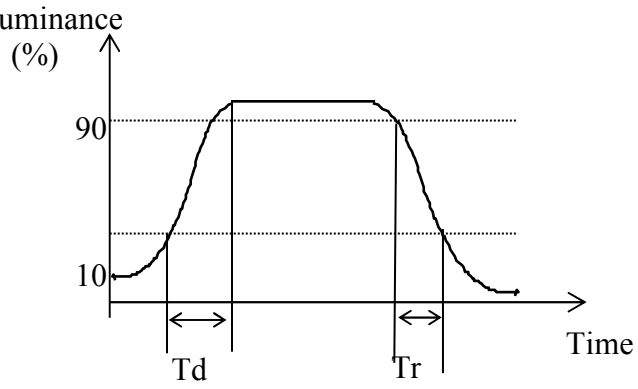
7.1 Electro-optical characteristics (at ambient temperature = 25°C)

NO	ITEM	SYMBOL	CONDITION	LCD TYPE UNIT	REF.
1.	Viewing Angle (Deg)	θ x 1	CR ≥ 250	50	7.1.2
		θ x 2		65	
		θ y 1		65	
		θ y 2		65	
2.	Contrast Ratio	CR	$\theta = 0^0$	800	7.1.3
3.	Response Time (msec)	Rise Time (Tr) + Decay Time (Td)	$\theta = 0^0$	35	7.1.4

*Note:

1. Viewing angle data is based on bottom view product by default. Should it be a top view product, values are then swap.
2. Contrast ratio is based on typical data when using white colour as backlight.
3. Equipment Used Eldim; Ez Contrast 120R , Spot Size = 2mm

NO	CHARACTERISTICS	DEFINITIONS
7.1.1	***Definition of Operating Voltage (V_{LCD})***	 V_{LCD} : Operating Voltage F : Frame Frequency
7.1.2	***Definition of Viewing Angle***	 

7.1.3	***Definition of Contrast Ratio***	 Contrast Ratio = Brightness of non-selected state (b) / Brightness of selected state (a) ***Conditions*** (a) Operating Voltage: V_{LCD} (b) Temperature: 25°C (c) Viewing Angle, θ = 0°
7.1.4	***Response Time***	 Tr: Measured between 10% and 90% of LCD segment maximum response with $V_{ON.}$ Td: With voltage switches to zero and the instant LCD segment reaches 10% of its maximum response.

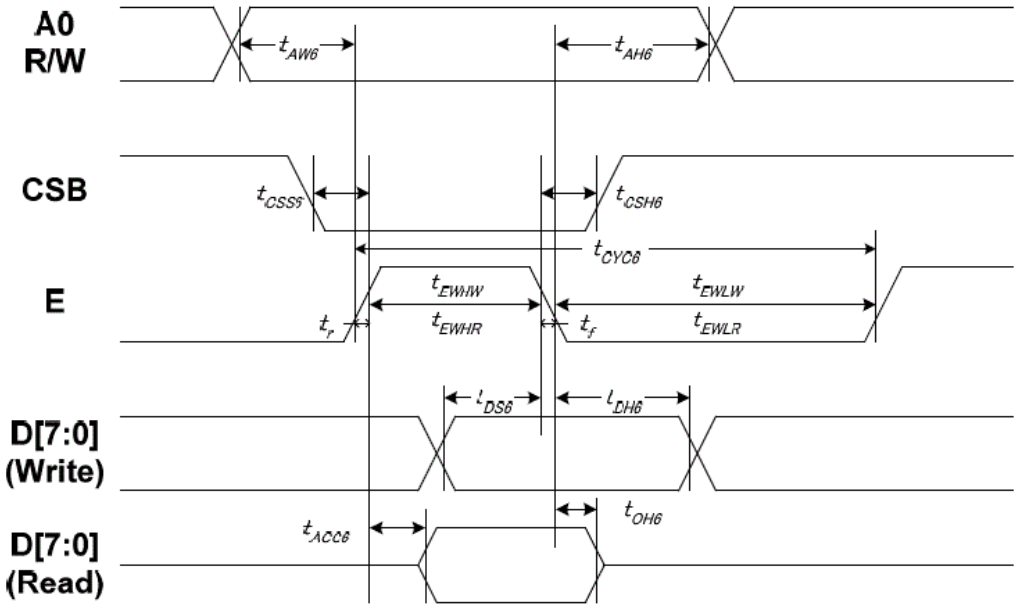
8.0 Interface

8.1	***Display Driver***	ST7511 or equivalent	
8.2	**Pin No**	**Symbol**	**Description**
	1	GND	Ground
	2	GND	Ground
	3	VDDA	Power supply for analog and booster circuit
	4	VDDI	Power supply for IO system
	5	D0 / SDA	8 bits bi-directional data bus / Serial data
	6	D1	8 bits bi-directional data bus
	7	D2	8 bits bi-directional data bus
	8	D3	8 bits bi-directional data bus
	9	D4	8 bits bi-directional data bus
	10	D5	8 bits bi-directional data bus
	11	D6	8 bits bi-directional data bus
	12	D7 / SCL	8 bits bi-directional data bus / Serial input clock
	13	RSTB	Reset input, active low
	14	CSB	Chip select input, active low
	15	A0	Register select input, H : Data / Parameter, L : Command
	16	RWR	R/W : 6800 Series Parallel Interface Read & Write Control Input /WR : 8080 Series Parallel Interface Write Enable Clock Input
	17	ERD	E : 6800 Series Parallel Interface Read & Write Control Input /RD : 8080 Series Parallel Interface Read Enable Clock Input
	18	NC	No Connection
	19	K	LED cathode
	20	A	LED anode

9.0 Functional Descriptions

9.1 Read/Write timing characteristics

System Bus Timing for 6800 Series MPU



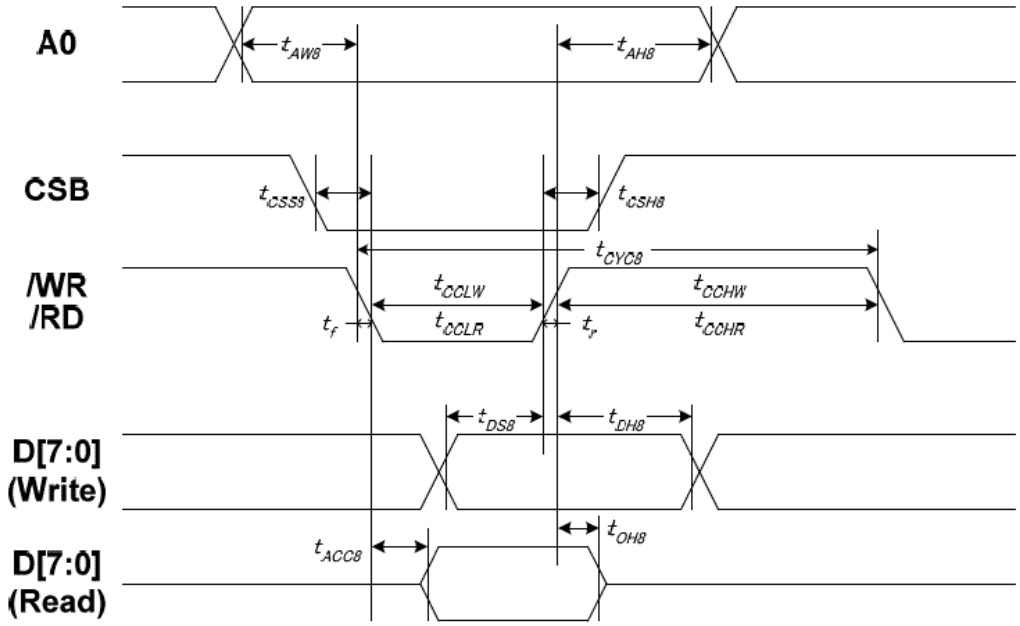
AGND = PGND =DGND = 0V, VDDA = VDDP= VDDI = 3.0 to 5.0V , Ta = 25℃

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW6		10	—	ns
Address hold time		tAH6		0	—	
System cycle time	E	tCYC6		1100	—	
Enable L pulse width (WRITE)		tEWLW		500	—	
Enable H pulse width (WRITE)		tEWHW		500	—	
Enable L pulse width (READ)		tEWLR		500	—	
Enable H pulse width (READ)		tEWHR		500	—	
CSB setup time	CSB	tCSS6		100	—	
CSB hold time		tCSH6		130	—	
Write data setup time	D[7:0]	tDS6		200	—	
Write data hold time		tDH6		250	—	
Read data access time		tACC6	CL = 100 pF	—	950	
Read data output disable time		tOH6	CL = 100 pF	5	200	

Note:

1. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) ≤ (tCYC8 – tCCLW – tCCHW) for (tr + tf) ≤ (tCYC8 – tCCLR – tCCHR) are specified.
2. All timing is specified using 20% and 80% of VDD1 as the reference.
3. tCCLW and tCCLR are specified as the overlap between CSB being “L” and /WR and /RD being at the “L” level. CSB and /WR (or /RD) cannot act at the same time and CSB should be 100ns widther than /WR (or /RD).

System Bus Timing for 8080 Series MPU



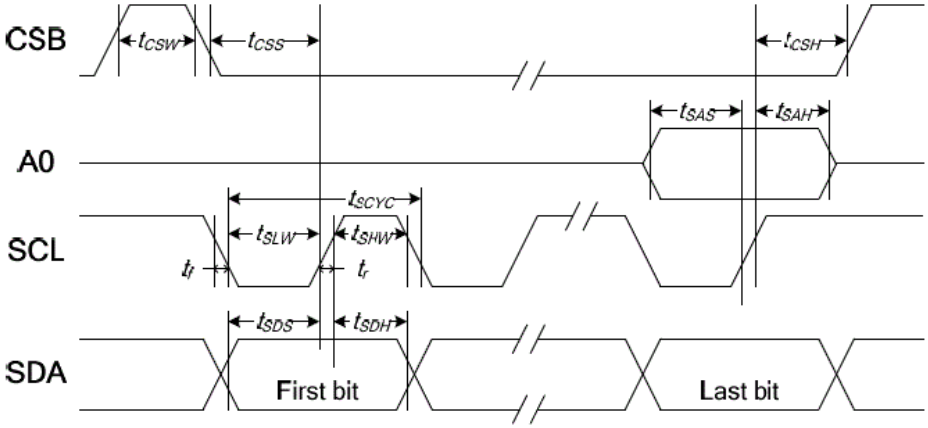
AGND = PGND =DGND = 0V, VDDA = VDDP= VDDI = 3.0 to 5.0V , Ta = 25℃

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW8		10	—	ns
Address hold time		tAH8		0	—	
System cycle time	/WR	tCYC8		1100	—	
/WR L pulse width (WRITE)		tCCLW		500	—	
/WR H pulse width (WRITE)		tCCHW		500	—	
/RD L pulse width (READ)	/RD	tCCLR		950	—	
/RD H pulse width (READ)		tCCHR		500	—	
CSB setup time	CSB	tCSS8		100	—	
CSB hold time		tCSH8		100	—	
WRITE Data setup time	D[7:0]	tDS8		200	—	
WRITE Data hold time		tDH8		50	—	
READ access time		tACC8	CL = 100 pF	—	950	
READ Output disable time		tOH8	CL = 100 pF	5	200	

Note:

1. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) ≤ (tCYC8 – tCCLW – tCCHW) for (tr + tf) ≤ (tCYC8 – tCCLR – tCCHR) are specified.
2. All timing is specified using 20% and 80% of VDD1 as the reference.
3. tCCLW and tCCLR are specified as the overlap between CSB being “L” and /WR and /RD being at the “L” level. CSB and /WR (or /RD) cannot act at the same time and CSB should be 100ns widther than /WR (or /RD).

System Bus Timing for 4-Line Serial Interface



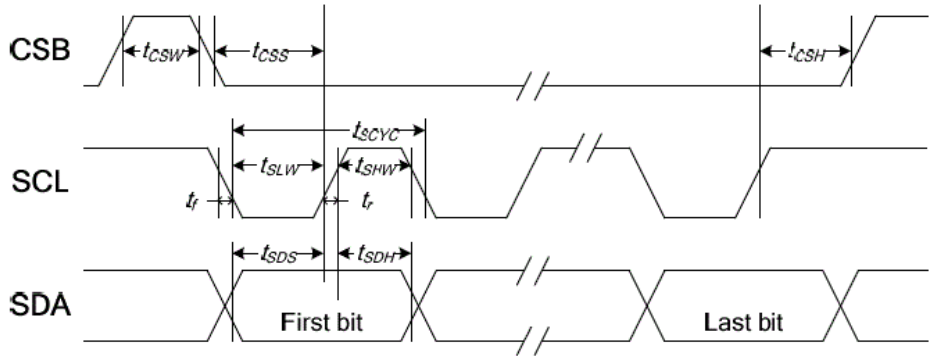
AGND = PGND =DGND = 0V, VDDA = VDDP= VDDI = 3.0 to 5.0V, Ta = 25℃

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCL	tSCYC		300	—	ns
SCL "H" pulse width		tSHW		150	—	
SCL "L" pulse width		tSLW		150	—	
Address setup time	A0	tSAS		150	—	
Address hold time		tSAH		150	—	
Data setup time	SDA	tSDS		120	—	
Data hold time		tSDH		120	—	
CSB-SCL time	CSB	tCSS		150	—	
CSB-SCL time		tCSH		150	—	
CSB "H" pulse width		tCSW		30	—	

Note:

1. The input signal rise and fall time (tr, tf) are specified at 15 ns or less.
2. All timing is specified using 20% and 80% of VDD1 as the standard.

System Bus Timing for 3-Line Serial Interface



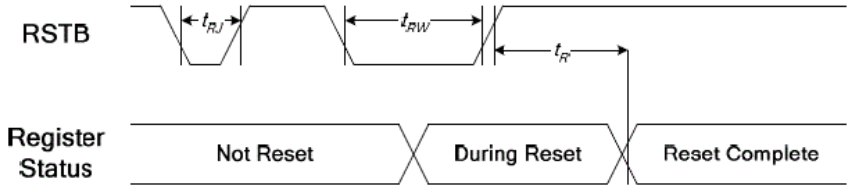
AGND = PGND =DGND = 0V, VDDA = VDDP= VDDI = 3.0 to 5.0V, Ta = 25℃

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial Clock Period	SCL	tSCYC		300	—	ns
SCL "H" pulse width		tSHW		150	—	
SCL "L" pulse width		tSLW		150	—	
Data setup time	SDA	tSDS		120	—	
Data hold time		tSDH		120	—	
CSB-SCL time	CSB	tCSS		150	—	
CSB-SCL time		tCSH		150	—	
CSB "H" pulse width		tCSW		30	—	

Note:

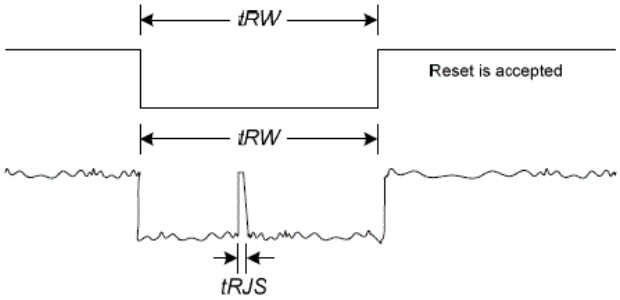
1. The input signal rise and fall time (tr, tf) are specified at 15 ns or less.
2. All timing is specified using 20% and 80% of VDD1 as the standard.

Hardware Reset Timing



AGND = PGND =DGND = 0V, VDDA = VDDP= VDDI = 3.0 to 5.0V, Ta = 25℃

Item	Signal	Symbol	Condition	Rating		Unit
				Min.	Max.	
Reset time	RSTB	tR		—	5 *1	us
Reset "L" pulse width		tRW		15	—	
Reset rejection		tRJ		—	5	
Reset rejection (for noise spike)		tRJS		—	10	ns

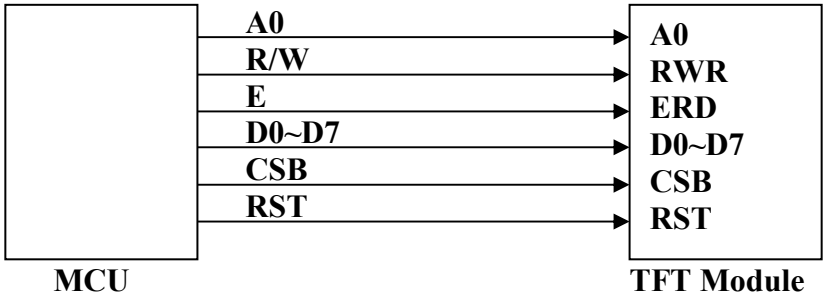


Note:

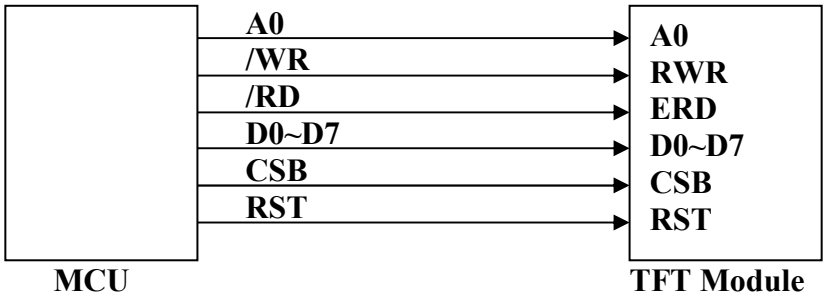
1. For PROM related operation, it takes 50ms at least for PROM Registers to load PROM contents. Do NOT use any PROM related command during this period.
2. When the system issues a RSTB LOW pulse, the reset procedure of IC will start if the LOW pulse is longer than tRW specified above. If the LOW pulse is less than tRJ specified above, the reset procedure of IC will not start. If the LOW pulse is longer than tRJ and less than tRW, the reset procedure of IC is not guaranteed.

9.2 Application Circuits

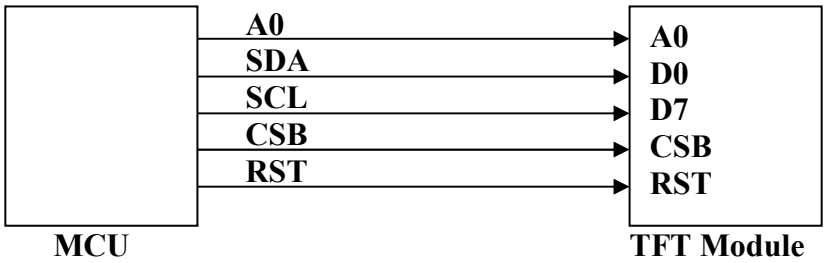
9.2.1 6800 – Series Parallel Interface



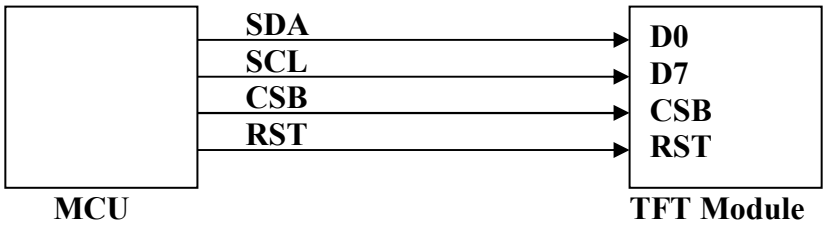
9.2.2 8080 – Series Parallel Interface



9.2.3 4-line Serial Interface



9.2.4 3-line Serial Interface



10.0 Instruction set

Instruction	Add. (hex)	A0	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	Default (hex)	Function
NOP	00	0	1	↑	0	0	0	0	0	0	0	0		Non-Operati
		1	1	↑	1	0	1	0	0	1	0	1		on
SLPOUT	12	0	1	↑	0	0	0	1	0	0	1	0		Sleep Out
		1	1	↑	1	0	1	0	0	1	0	1		
SLPIN	13	0	1	↑	0	0	0	1	0	0	1	1		Sleep In
		1	1	↑	1	0	1	0	0	1	0	1		
DISOFF	14	0	1	↑	0	0	0	1	0	1	0	0		Display Off
		1	1	↑	1	0	1	0	0	1	0	1		
DISON	15	0	1	↑	0	0	0	1	0	1	0	1		Display On
		1	1	↑	1	0	1	0	0	1	0	1		
DINVOUT	1A	0	1	↑	0	0	0	1	1	0	1	0		Display
		1	1	↑	1	0	1	0	0	1	0	1		Invert Out
DINVIN	1B	0	1	↑	0	0	0	1	1	0	1	1		Display
		1	1	↑	1	0	1	0	0	1	0	1		Invert In
BLOUT	1C	0	1	↑	0	0	0	1	1	1	0	0		Blinking Out
		1	1	↑	1	0	1	0	0	1	0	1		
BLIN	1D	0	1	↑	0	0	0	1	1	1	0	1		Blinking In
		1	1	↑	1	0	1	0	0	1	0	1		
STFRAME	21	0	1	↑	0	0	1	0	0	0	0	1		Start Frame Address
		1	1	↑	0	0	0	0	0	0	SFrmA1	SFrmA0	00	
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
BPPSEL	22	0	1	↑	0	0	1	0	0	0	1	0		BPP Select
		1	1	↑	0	0	0	0	0	0	BppSel1	BppSel0	02	
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
MADCTL	24	0	1	↑	0	0	1	0	0	1	0	0		Memory Address Control
		1	1	↑	0	0	0	0	0	MV	MY	MX	00	
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
PASET	25	0	1	↑	0	0	1	0	0	1	0	1		Page Address Set
		1	1	↑	PSA7	PSA6	PSA5	PSA4	PSA3	PSA2	PSA1	PSA0	00	
		1	1	↑	PEA7	PEA6	PEA5	PEA4	PEA3	PEA2	PEA1	PEA0	9F	
		1	1	↑	0	0	0	0	0	0	FrmA1	FrmA0	00	
		1	1	↑	1	0	1	0	0	1	0	1		
CASET	26	0	1	↑	0	0	1	0	0	1	1	0		Column

		1	1	↑	0	0	0	0	0	0	CSA9	CSA8	00	Address Set
		1	1	↑	CSA7	CSA6	CSA5	CSA4	CSA3	CSA2	CSA1	CSA0	00	
		1	1	↑	0	0	0	0	0	0	CEA9	CEA8	02	
		1	1	↑	CEA7	CEA6	CEA5	CEA4	CEA3	CEA2	CEA1	CEA0	7F	
BLKFIL	29	0	1	↑	0	0	1	0	1	0	0	1		Block Fill
		1	1	↑	0	0	0	0	BFData3	BFData2	BFData1	BFData0	00	
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
BLSET	2B	0	1	↑	0	0	1	0	1	0	1	1		Blinking Set
		1	1	↑	BlinkCyc7	BlinkCyc6	BlinkCyc5	BlinkCyc4	BlinkCyc3	BlinkCyc2	BlinkCyc1	BlinkCyc0	1D	
		1	1	↑	0	0	0	0	B1stF1	B1stF0	B2ndF1	B2ndF0	01	
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
WRRAM	2C	0	1	↑	0	0	1	0	1	1	0	0		Write RAM
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0		
RDRAM	2D	0	1	↑	0	0	1	0	1	1	0	1		Read RAM
		1	1	↑	1	0	1	0	0	1	0	1		
		1	↑	1	X	X	X	X	X	X	X	X		
		1	↑	1	Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0		
DISAR	31	0	1	↑	0	0	1	1	0	0	0	1		Display Area
		1	1	↑	0	0	0	0	0	0	0	DisLin8	01	
		1	1	↑	DisLin7	DisLin6	DisLin5	DisLin4	DisLin3	DisLin2	DisLin1	DisLin0	3F	
		1	1	↑	0	0	0	0	0	0	DisCol9	DisCol8	02	
		1	1	↑	DisCol7	DisCol6	DisCol5	DisCol4	DisCol3	DisCol2	DisCol1	DisCol0	7F	
DISSET1	32	0	1	↑	0	0	1	1	0	0	1	0		Display Set1
		1	1	↑	HClkNo7	HClkNo6	HClkNo5	HClkNo4	HClkNo3	HClkNo2	HClkNo1	HClkNo0	32	
		1	1	↑	BPNo7	BPNo6	BPNo5	BPNo4	BPNo3	BPNo2	BPNo1	BPNo0	02	
		1	1	↑	NorBlk	OSCO	0	0	FPNo11	FPNo10	FPNo9	FPNo8	00	
		1	1	↑	FPNo7	FPNo6	FPNo5	FPNo4	FPNo3	FPNo2	FPNo1	FPNo0	01	
DISSET2	33	0	1	↑	0	0	1	1	0	0	1	1		Display Set2
		1	1	↑	SOnT7	SOnT6	SOnT5	SOnT4	SOnT3	SOnT2	SOnT1	SOnT0	0A	
		1	1	↑	SOffT7	SOffT6	SOffT5	SOffT4	SOffT3	SOffT2	SOffT1	SOffT0	28	
		1	1	↑	GOnT7	GOnT6	GOnT5	GOnT4	GOnT3	GOnT2	GOnT1	GOnT0	0C	
		1	1	↑	GOffT7	GOffT6	GOffT5	GOffT4	GOffT3	GOffT2	GOffT1	GOffT0	26	
PTLSET1	34	0	1	↑	0	0	1	1	0	1	0	0		Partial Set 1
		1	1	↑	0	0	0	0	0	0	0	Part1SL8	00	
		1	1	↑	Part1SL7	Part1SL6	Part1SL5	Part1SL4	Part1SL3	Part1SL2	Part1SL1	Part1SL0	00	
		1	1	↑	0	0	0	0	0	0	0	Part1EL8	00	
		1	1	↑	Part1EL7	Part1EL6	Part1EL5	Part1EL4	Part1EL3	Part1EL2	Part1EL1	Part1EL0	00	
PTLSET2	35	0	1	↑	0	0	1	1	0	1	0	1		Partial Set 2
		1	1	↑	0	0	0	0	0	0	0	Part2SL8	00	
		1	1	↑	Part2SL7	Part2SL6	Part2SL5	Part2SL4	Part2SL3	Part2SL2	Part2SL1	Part2SL0	00	
		1	1	↑	0	0	0	0	0	0	0	Part2EL8	00	

		1	1	↑	Part2EL7	Part2EL6	Part2EL5	Part2EL4	Part2EL3	Part2EL2	Part2EL1	Part2EL0	00	
PTLSET3	36	0	1	↑	0	0	1	1	0	1	1	0		Partial Set 3
		1	1	↑	0	NDisRefR6	NDisRefR5	NDisRefR4	NDisRefR3	NDisRefR2	NDisRefR1	NDisRefR0	00	
		1	1	↑	0	0	0	0	0	RTBFreq2	RTBFreq1	RTBFreq0	00	
		1	1	↑	0	0	0	0	0	0	NDisDM1	NDisDM0	00	
		1	1	↑	1	0	1	0	0	1	0	1		
VCMDAT	54	0	1	↑	0	1	0	1	0	1	0	0		VCOM Offset Data
		1	1	↑	0	0	0	0	VcomS3	VcomS2	VcomS1	VcomS0	00	
		1	1	↑	0	0	VcomD15	VcomD14	VcomD13	VcomD12	VcomD11	VcomD10	00	
		1	1	↑	0	0	VcomD25	VcomD24	VcomD23	VcomD22	VcomD21	VcomD20	00	
		1	1	↑	1	0	1	0	0	1	0	1		
UIDSET	55	0	1	↑	0	1	0	1	0	1	0	1		User ID
		1	1	↑	UID117	UID116	UID115	UID114	UID113	UID112	UID111	UID110	00	
		1	1	↑	UID127	UID126	UID125	UID124	UID123	UID122	UID121	UID120	00	
		1	1	↑	UID217	UID216	UID215	UID214	UID213	UID212	UID211	UID210	00	
		1	1	↑	UID227	UID226	UID225	UID224	UID223	UID222	UID221	UID220	00	
MTPMOD	5A	0	1	↑	0	1	0	1	1	0	1	0		Multi Time PROM Mode
		1	1	↑	MTPMOD7	MTPMOD6	MTPMOD5	MTPMOD4	MTPMOD3	MTPMOD2	MTPMOD1	MTPMOD0	00	
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
MTPOP	5B	0	1	↑	0	1	0	1	1	0	1	1		Multi Time PROM Operation
		1	1	↑	0	0	0	0	0	MTP_Sel	0	Prog_Mod	00	
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
PWRCTL	61	0	1	↑	0	1	1	0	0	0	0	1		Power Control
		1	1	↑	BST3SR1	BST3SR0	0	0	BST4ON	BST3ON	BST2ON	BST1ON	40	
		1	1	↑	FOFNo3	FOFNo2	FOFNo1	FOFNo0	0	SAMPSet2	SAMPSet1	SAMPSet0	01	
		1	1	↑	0	0	0	0	0	0	1	0	02	
		1	1	↑	1	0	1	0	0	1	0	1		
EVSET1	62	0	1	↑	0	1	1	0	0	0	1	0		Electronic Volumn Set 1
		1	1	↑	0	VCOM6	VCOM5	VCOM4	VCOM3	VCOM2	VCOM1	VCOM0	0A	
		1	1	↑	0	0	VGHREG5	VGHREG4	VGHREG3	VGHREG2	VGHREG1	VGHREG0	06	
		1	1	↑	0	0	0	VGLREG4	VGLREG3	VGLREG2	VGLREG1	VGLREG0	0F	
		1	1	↑	1	0	1	0	0	1	0	1		
EVSET2	63	0	1	↑	0	1	1	0	0	0	1	1		Electronic Volumn Set 2
		1	1	↑	0	0	0	GVDD4	GVDD3	GVDD2	GVDD1	GVDD0	0F	
		1	1	↑	0	0	0	GVCL4	GVCL3	GVCL2	GVCL1	GVCL0	0F	
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
BCLKSET	64	0	1	↑	0	1	1	0	0	1	0	0		Booster Clock Setting
		1	1	↑	0	AVclClk2	AVclClk1	AVclClk0	0	AVdClk2	AVdClk2	AVdClk2	44	
		1	1	↑	0	VglClk2	VglClk1	VglClk0	0	Vghclk2	Vghclk1	VghClk0	44	
		1	1	↑	0	AVclClk_nd2	AVdClk_nd1	AVclClk_nd2	0	AVdClk_nd2	AVdClk_nd1	AVdClk_nd0	44	

		1	1	↑	0	VglClk_nd2	VglClk_nd1	VglClk_nd0	0	VghdIk_nd2	VghcIk_nd1	VghClk_nd0	44	
GATESET	66	0	1	↑	0	1	1	0	0	1	1	0		Gate Set
		1	1	↑	VGPP	0	0	ScanDir	0	0	ScanMod1	ScanMod0	00	
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
PWMCTRL	6C	0	1	↑	0	1	1	0	1	1	0	0		PWM Control
		1	1	↑	0	0	0	0	0	LOnTyp	0	LEDMD	00	
		1	1	↑	SLEDOn7	SLEDOn6	SLEDOn5	SLEDOn4	SLEDOn3	SLEDOn2	SLEDOn1	SLEDOn0		
		1	1	↑	ASLEDOn7	ASLEDOn6	ASLEDOn5	ASLEDOn4	ASLEDOn3	ASLEDOn2	ASLEDOn1	ASLEDOn0		
		1	1	↑	ASLEDOf7	ASLEDOf6	ASLEDOf5	ASLEDOf4	ASLEDOf3	ASLEDOf2	ASLEDOf1	ASLEDOf0		
RDSTAT	72	0	1	↑	0	1	1	1	0	0	1	0		Read Status
		1	1	↑	1	0	1	0	0	1	0	1		
		1	↑	1	R17	R16	R15	0	R13	R12	R11	R10		
		1	↑	1	0	R26	R25	R24	R23	R22	R21	R20		
		1	↑	1	R37	R36	R35	R34	R33	R32	R31	R30		
		1	↑	1	R47	R46	R45	R44	R43	R42	R41	R40		
		1	↑	1	0	0	0	0	0	R52	R51	R50		
		1	↑	1	0	R66	R65	R64	0	R62	R61	R60		
RDREV	73	0	1	↑	0	1	1	1	0	0	1	1		Read Revision
		1	1	↑	1	0	1	0	0	1	0	1		
		1	↑	1	R17	R16	R15	R14	R13	R12	R11	R10		
RDUID	75	0	1	↑	0	1	1	1	0	1	0	1		Read User ID
		1	1	↑	1	0	1	0	0	1	0	1		
		1	↑	1	R17	R16	R15	R14	R13	R12	R11	R10		
		1	↑	1	R27	R26	R25	R24	R23	R22	R21	R20		
		1	↑	1	R37	R36	R35	R34	R33	R32	R31	R30		
		1	↑	1	R47	R46	R45	R44	R43	R42	R41	R40		
		1	↑	1	R57	R56	R55	R54	R53	R52	R51	R50		
		1	↑	1	R67	R66	R65	R64	R63	R62	R61	R60		
		1	↑	1	R77	R76	R75	R74	R73	R72	R71	R70		
		1	↑	1	R87	R86	R85	R84	R83	R82	R81	R80		
		1	↑	1	R97	R96	R95	R94	R93	R92	R91	R90		
		1	↑	1	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0		
		1	↑	1	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0		
		1	↑	1	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0		
RDVCMDAT	79	0	1	↑	0	1	1	1	1	0	0	1		Read VCOM Data
		1	1	↑	1	0	1	0	0	1	0	1		
		1	↑	1	x	x	R15	R14	R13	R12	R11	R10		
		1	↑	1	x	x	R25	R24	R23	R22	R21	R20		
		1	↑	1	x	x	R35	R34	R33	R32	R31	R30		
		1	↑	1	x	x	R45	R44	R43	R42	R41	R40		
		1	↑	1	x	x	R55	R54	R53	R52	R51	R50		
		1	↑	1	x	x	R65	R64	R63	R62	R61	R60		
		1	↑	1	x	x	R75	R74	R73	R72	R71	R70		

		1	↑	1	0	0	0	0	R83	R82	R81	R80		
GAMSET4 P1	91	0	1	↑	1	0	0	1	0	0	0	1		Gamma Set 4bpp Positive 1
		1	1	↑	0	0	G4BPV05	G4BPV04	G4BPV03	G4BPV02	G4BPV01	G4BPV00	00	
		1	1	↑	0	0	G4BPV15	G4BPV14	G4BPV13	G4BPV12	G4BPV11	G4BPV10	04	
		1	1	↑	0	0	G4BPV25	G4BPV24	G4BPV23	G4BPV22	G4BPV21	G4BPV20	08	
		1	1	↑	0	0	G4BPV35	G4BPV34	G4BPV33	G4BPV32	G4BPV31	G4BPV30	0C	
GAMSET4 P2	92	0	1	↑	1	0	0	1	0	0	1	0		Gamma Set 4bpp Positive 2
		1	1	↑	0	0	G4BPV45	G4BPV44	G4BPV43	G4BPV42	G4BPV41	G4BPV40	10	
		1	1	↑	0	0	G4BPV55	G4BPV54	G4BPV53	G4BPV52	G4BPV51	G4BPV50	14	
		1	1	↑	0	0	G4BPV65	G4BPV64	G4BPV63	G4BPV62	G4BPV61	G4BPV60	18	
		1	1	↑	0	0	G4BPV75	G4BPV74	G4BPV73	G4BPV72	G4BPV71	G4BPV70	1C	
GAMSET4 P3	93	0	1	↑	1	0	0	1	0	0	1	1		Gamma Set 4bpp Positive 3
		1	1	↑	0	0	G4BPV85	G4BPV84	G4BPV83	G4BPV82	G4BPV81	G4BPV80	23	
		1	1	↑	0	0	G4BPV95	G4BPV94	G4BPV93	G4BPV92	G4BPV91	G4BPV90	27	
		1	1	↑	0	0	G4BPVA5	G4BPVA4	G4BPVA3	G4BPVA2	G4BPVA1	G4BPVA0	2B	
		1	1	↑	0	0	G4BPVB5	G4BPVB4	G4BPVB3	G4BPVB2	G4BPVB1	G4BPVB0	2F	
GAMSET4 P4	94	0	1	↑	1	0	0	1	0	1	0	0		Gamma Set 4bpp Positive 4
		1	1	↑	0	0	G4BPVC5	G4BPVC4	G4BPVC3	G4BPVC2	G4BPVC1	G4BPVC0	33	
		1	1	↑	0	0	G4BPVD5	G4BPVD4	G4BPVD3	G4BPVD2	G4BPVD1	G4BPVD0	37	
		1	1	↑	0	0	G4BPVE5	G4BPVE4	G4BPVE3	G4BPVE2	G4BPVE1	G4BPVE0	3B	
		1	1	↑	0	0	G4BPVF5	G4BPVF4	G4BPVF3	G4BPVF2	G4BPVF1	G4BPVF0	3F	
GAMSET2 P	95	0	1	↑	1	0	0	1	0	1	0	1		Gamma Set 2bpp Positive
		1	1	↑	0	0	G2BPV05	G2BPV04	G2BPV03	G2BPV02	G2BPV01	G2BPV00	00	
		1	1	↑	0	0	G2BPV15	G2BPV14	G2BPV13	G2BPV12	G2BPV11	G2BPV10	15	
		1	1	↑	0	0	G2BPV25	G2BPV24	G2BPV23	G2BPV22	G2BPV21	G2BPV20	2A	
		1	1	↑	0	0	G2BPV35	G2BPV34	G2BPV33	G2BPV32	G2BPV31	G2BPV30	3F	
GAMSET1	96	0	1	↑	1	0	0	1	0	1	1	0		Gamma Set 1bpp
		1	1	↑	0	0	G1BPV05	G1BPV04	G1BPV03	G1BPV02	G1BPV01	G1BPV00	00	
		1	1	↑	0	0	G1BPV15	G1BPV14	G1BPV13	G1BPV12	G1BPV11	G1BPV10	3F	
		1	1	↑	0	0	G1BNV05	G1BNV04	G1BNV03	G1BNV02	G1BNV01	G1BNV00	00	
		1	1	↑	0	0	G1BNV15	G1BNV14	G1BNV13	G1BNV12	G1BNV11	G1BNV10	3F	
GAMSET4 N1	99	0	1	↑	1	0	0	1	1	0	0	1		Gamma Set 4bpp Negative 1
		1	1	↑	0	0	G4BNV05	G4BNV04	G4BNV03	G4BNV02	G4BNV01	G4BNV00	00	
		1	1	↑	0	0	G4BNV15	G4BNV14	G4BNV13	G4BNV12	G4BNV11	G4BNV10	04	
		1	1	↑	0	0	G4BNV25	G4BNV24	G4BNV23	G4BNV22	G4BNV21	G4BNV20	08	
		1	1	↑	0	0	G4BNV35	G4BNV34	G4BNV33	G4BNV32	G4BNV31	G4BNV30	0C	
GAMSET4 N2	9A	0	1	↑	1	0	0	1	1	0	1	0		Gamma Set 4bpp Negative 2
		1	1	↑	0	0	G4BNV45	G4BNV44	G4BNV43	G4BNV42	G4BNV41	G4BNV40	10	
		1	1	↑	0	0	G4BNV55	G4BNV54	G4BNV53	G4BNV52	G4BNV51	G4BNV50	14	
		1	1	↑	0	0	G4BNV65	G4BNV64	G4BNV63	G4BNV62	G4BNV61	G4BNV60	18	
		1	1	↑	0	0	G4BNV75	G4BNV74	G4BNV73	G4BNV72	G4BNV71	G4BNV70	1C	
GAMSET4 N3	9B	0	1	↑	1	0	0	1	1	0	1	1		Gamma Set 4bpp Negative 3
		1	1	↑	0	0	G4BNV85	G4BNV84	G4BNV83	G4BNV82	G4BNV81	G4BNV80	23	
		1	1	↑	0	0	G4BNV95	G4BNV94	G4BNV93	G4BNV92	G4BNV91	G4BNV90	27	
		1	1	↑	0	0	G4BNVA5	G4BNVA4	G4BNVA3	G4BNVA2	G4BNVA1	G4BNVA0	2B	

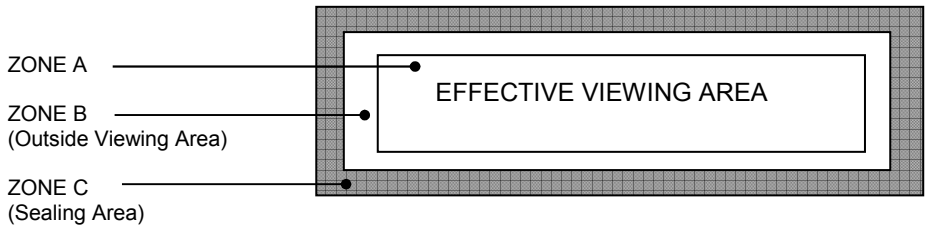
		1	1	↑	0	0	G4BNVB5	G4BNVB4	G4BNVB3	G4BNVB2	G4BNVB1	G4BNVB0	2F	
GAMSET4N4	9C	0	1	↑	1	0	0	1	1	1	0	0		Gamma Set 4bpp Negative 4
		1	1	↑	0	0	G4BNVC5	G4BNVC4	G4BNVC3	G4BNVC2	G4BNVC1	G4BNVC0	33	
		1	1	↑	0	0	G4BNVD5	G4BNVD4	G4BNVD3	G4BNVD2	G4BNVD1	G4BNVD0	37	
		1	1	↑	0	0	G4BNVE5	G4BNVE4	G4BNVE3	G4BNVE2	G4BNVE1	G4BNVE0	3B	
		1	1	↑	0	0	G4BNVF5	G4BNVF4	G4BNVF3	G4BNVF2	G4BNVF1	G4BNVF0	3F	
GAMSET2N	9D	0	1	↑	1	0	0	1	1	1	0	1		Gamma Set 2bpp Negative
		1	1	↑	0	0	G2BNV05	G2BNV04	G2BNV03	G2BNV02	G2BNV01	G2BNV00	00	
		1	1	↑	0	0	G2BNV15	G2BNV14	G2BNV13	G2BNV12	G2BNV11	G2BNV10	15	
		1	1	↑	0	0	G2BNV25	G2BNV24	G2BNV23	G2BNV22	G2BNV21	G2BNV20	2A	
		1	1	↑	0	0	G2BNV35	G2BNV34	G2BNV33	G2BNV32	G2BNV31	G2BNV30	3F	
RMWIN	A1	0	1	↑	1	0	1	0	0	0	0	1		Read Modify Write In
		1	1	↑	1	0	1	0	0	1	0	1		
MTPRDEN	A2	0	1	↑	1	0	1	0	0	0	1	0		MTP Read Enable
		1	1	↑	1	0	1	0	0	1	0	1		
MTPWREN	A3	0	1	↑	1	0	1	0	0	0	1	1		MTP Write Enable
		1	1	↑	1	0	1	0	0	1	0	1		
PTLOUT	A9	0	1	↑	1	0	1	0	1	0	0	1		Partial Out
		1	1	↑	1	0	1	0	0	1	0	1		
PTLIN	AA	0	1	↑	1	0	1	0	1	0	1	0		Partial In
		1	1	↑	1	0	1	0	0	1	0	1		
RMWOUT	AC	0	1	↑	1	0	1	0	1	1	0	0		Read Modify Write Out
		1	1	↑	1	0	1	0	0	1	0	1		
SWRESET	AE	0	1	↑	1	0	1	0	1	1	1	0		Software Reset
		1	1	↑	1	0	1	0	0	1	0	1		

10.1 Initialization code for ST7511

```
WrCommand(0xAE);   // SWreset
WrData(0xA5);

WrCommand(0x61);   // all PWR ON
WrData(0x0F);
WrData(0x04);
WrData(0xA5);
WrData(0xA5);

WrCommand(0x62);   // Electronic Volumn Set 1
WrData(0x0A);      // VCOM[6:0] 0~127 => -0.4250-(0.0125xVCOM)
WrData(0x06);      // VGHREG[5:0] 0~63 => 1.5+(0.1x(VGHREG-1))***
WrData(0x0F);      // VGLREG[4:0] 0~31 => 2.4+(0.1xVGLREG)
WrData(0xA5);

WrCommand(0x63);   // Electronic Volumn Set 2
WrData(0x0F);      // GVDD[4:0] 0~31 => 3.1+(0.1xGVDD)
WrData(0x0F);      // GVCL[4:0] 0~31 => -3.1-(0.1xGVCL)
WrData(0xA5);
WrData(0xA5);

WrCommand(0x66);   // Gate Set
WrData(0x01);  // VGPP:inside, ScanDir:normal, ScanMode:1/2/3/4
WrData(0xA5);
WrData(0xA5);
WrData(0xA5);

WrCommand(0x12);   // SLP out
WrData(0xA5);

WrCommand(0x24);   // mem address control
WrData(0x07); // MV,MY,MX
WrData(0xA5);
WrData(0xA5);
WrData(0xA5);
__delay_ms(1);

WrCommand(0x14);   // display OFF
WrData(0xA5);
WrCommand(0x22);   // BPP select
WrData(0x02);
WrData(0xA5);
WrData(0xA5);
WrData(0xA5);
WrCommand(0x15);   // display ON
WrData(0xA5);
```

11.0 Quality Assurance

11.1 Zone Definition

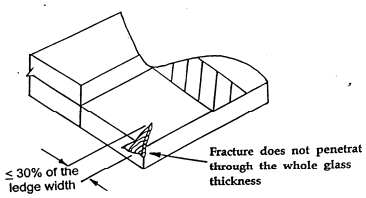


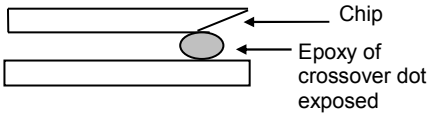
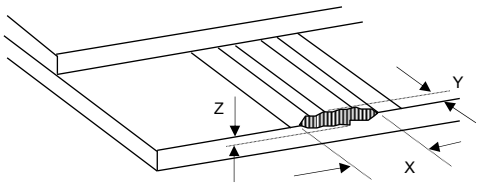
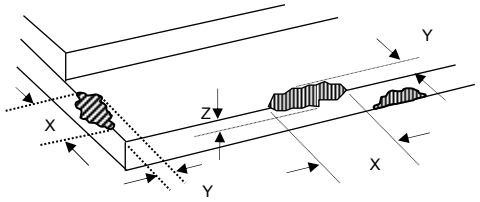
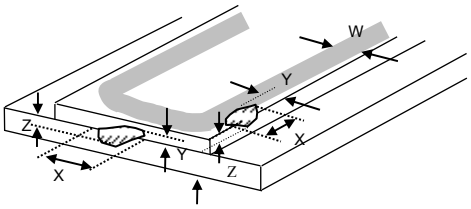
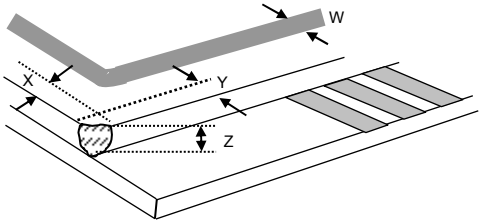
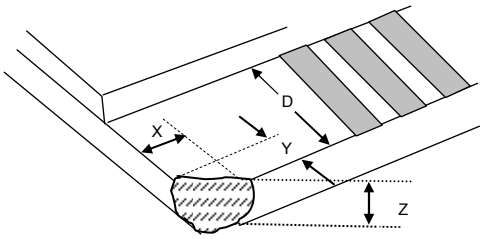
11.2 Rejection Criteria

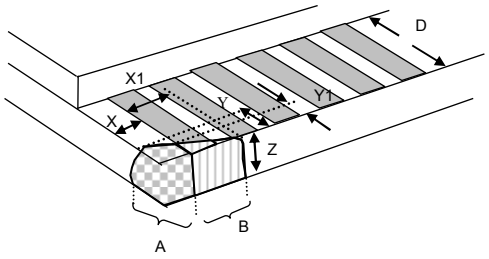
11.2.1 Dimensional Defects

Defect Category	Defect Description	Criterion	Drawing Specification
Glass Size	Dimensions of LCD, do not conform to the drawing	Reject	Refer to LCD Physical Dimension Drawing
Perimeter Seal Extension	Perimeter seal epoxy enters the effective viewing area	Reject	
End Seal Size	Size of end seal does not meet drawing specification	Reject	Refer to LCD Physical Dimension Drawing

11.2.2 Visual Defects

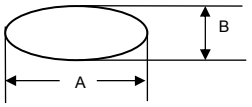
Defect Category	Defect Description	Criterion	Drawing Specification
Fracture	A type of glass breakage containing running cracks. Inspectors should attempt to remove it with fingernail. If removed, evaluate as chip	Reject – if the size is $\geq$ 30% of the contact ledge width.	

Defect Category	Defect Description	Criterion	Drawing Specification
Chip	Chip in cross over area	1) Reject - if the chip causes crossover dot to be exposed 2) Chip on outside edge of the glass plate but is greater than 50% of glass thickness at crossover dot is reject able.	
Chip	Chip in contact pad area	Accept if:- a) X ≤ 2.0mm b) Y ≤ 0.5mm c) Z disregard	
	Chip in non-contact pad area	Accept if:- a) X ≤ 6.0mm b) Y ≤ 1.0mm c) Z disregard	
	Chip in perimeter seal area	Accept if:- a) Y ≤ 1/3 of perimeter seal width (W) b) X ≤ 3.0mm c) Z disregard d) X and Y not touch crossover dot	
Corner Chip	Corner chip within seal area	Accept if:- a) X ≤ 1/3 of perimeter seal width (W) b) Y ≤ 1/3 of perimeter seal width (W) c) Z disregard	
	Corner chip not effecting contact pad / ITO	Accept if:- a) XY ≤ 4mm^2 AND b) Y ≤ D and X ≤ 2.0mm c) Z disregard	

Defect Category	Defect Description	Criterion	Drawing Specification
	Corner chip effecting contact pad / ITO	A) Accept if:- a) XY ≤ 4mm^2 AND b) Y ≤ D and X ≤ 2.0mm B) Accept if:- a) X1 ≤ 2.0mm b) Y1 ≤ 0.5mm Z disregard	
Glass flare	A thin layer of glass flare at contact area	Accept if:- a) Flare thickness ≤ ¼ W when W ≤ 3mm b) Flare thickness ≤ 1mm when W > 3mm W: Contact ledge width	
Glass burr	A rough edge(s) left along the scribing edge (i.e. along the edges of display)	Reject – if the burr cause undersize or oversize of the LCD	Refer to LCD Physical Dimension Drawing
Rainbow	Colored ring in sharp blotches observed	Reject – if 3 or more colored rings in sharp blotches of color are observed. (Limit samples should be used when applicable)	
Discoloration		Reject - if the discolorations enter the active viewing area of LCD. Color of the LCD shall follow product specification as specified in the manufacturing specification	
Air Void	LC does not fulfill the display	Reject	
Fill end contamination	Discoloration at end seal area	Reject if discoloration exceeded the baffle (for display with baffle) or viewing area (for display without baffle)	

11.2.3 Polarizer Defects

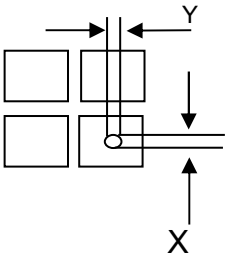
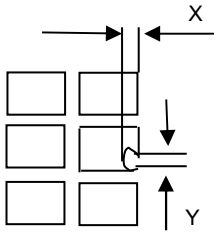
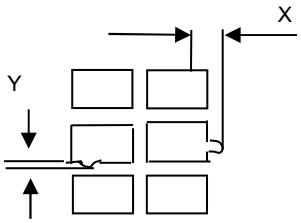
<table>
<tr><th>Defect Category</th><th>Defect Description</th><th>Criterion</th><th>Drawing Specification</th></tr>
<tr><td rowspan="5">Polarizer defect</td><td>Polarizer coverage</td><td>1- Polarizer should cover effective viewing area of display.
2- It is acceptable if perimeter seal bolder at all sides could be seen.
3- It is acceptable if polarizer attaching position meeting the tolerance mentioned in the drawing.
4- It is reject able if polarizer edge jagged and not even</td><td>Refer to LCD Physical Dimension Drawing</td></tr>
<tr><td>Polarizer Peeling / delamination</td><td>1- Reject if any edge or corner of the polarizer is lifted up or not adheres to the glass</td><td></td></tr>
<tr><td>Polarizer Scratches</td><td>1- Any scratch should be acceptable if it is not visible from viewing distance at head of position
2-Polarizer scratch in viewing area is reject able if it is visible from the specified viewing distance
3-Defect, which is visible under surface glare, should be disregard</td><td></td></tr>
<tr><td>Polarizer damage</td><td>1-Stain mark or depression in front polarizer surface should be acceptable if it is not visible from viewing distance at head on position.
2-Defect, which is visible under surface glare, should be disregard</td><td></td></tr>
<tr><td>Polarizer bubble / Foreign material</td><td>
<table>
<tr><td>Zone / Dimension</td><td colspan="2">Acceptable No.</td><td></td></tr>
<tr><td></td><td>A</td><td>B</td><td>C</td></tr>
<tr><td>D ≤ 0.30mm</td><td>NC</td><td>NC</td><td rowspan="4">NC if the Polarizer not lifted up/ peel off</td></tr>
<tr><td>D ≤ 0.50mm</td><td>2</td><td>NC</td></tr>
<tr><td>0.50 < D ≤ 0.60mm</td><td>1</td><td>2</td></tr>
<tr><td>D > 0.60mm</td><td>0</td><td>0</td></tr>
</table>
NC: No count
D: Mean Diameter of Defect

3 are the totally permissible numbers of bubble</td><td> 

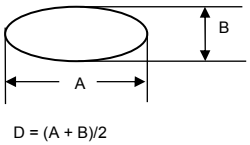
D = (A + B)/2</td></tr>
</table>

11.2.4 Electrical Test Defects

Defect Category	Defect Description	Criterion	Drawing Specification
Missing common	Part of the pattern does not light up	Reject	
Missing segment	One or few segment does not light up	Reject	
Common-common short	Common and common connected	Reject	

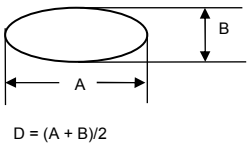
<table>
<tr><td>Segment-segment short</td><td>Segment and segment connected</td><td>Reject</td><td></td></tr>
<tr><td>Common – segment short</td><td>Common and segment connected</td><td>Reject</td><td></td></tr>
<tr><td>Wrong viewing angle</td><td>Wrong viewing angle</td><td>Reject if display viewing angle not conform to customer requirement</td><td></td></tr>
<tr><td>Metal residue</td><td>Extra spot lights up at the border of the segment.</td><td>Accept if ≤ 0.20mm (mean diameter)</td><td></td></tr>
<tr><td>Slow response</td><td>Response of the display on one side slower than the other side</td><td>Reject if it is visible at 30cm distance</td><td></td></tr>
<tr><td>Pin Hole</td><td>Pin hole / void at light up segment</td><td><table><tr><td>Zone / Dimension</td><td>Acceptable No.</td></tr><tr><td>Located inside single pixel/dot:- (X + Y)/2 ≤ 0.20mm</td><td>- 1 per pixel/dot
- 3 per display (Active Area)</td></tr><tr><td>Laid over the plural pixel/dots: (X + Y)/2 ≤ 0.20mm</td><td>- 1 per pixel/dot
- 3 per display (Active Area)</td></tr><tr><td colspan="2">(¾ or larger part of dot area has to be effective for display)</td></tr></table></td><td>  </td></tr>
<tr><td rowspan="2">Deformed display dot</td><td>Lacked deformation</td><td>Accept if:
i) X ≤ 0.15 and
ii) Y ≤ 0.15</td><td>  </td></tr>
<tr><td>Added deformation</td><td>Accept if:
i) X < 0.02 and
ii) Y < 0.02</td><td>  </td></tr>
<tr><td>Reverse twist/ tilt</td><td>Segment are darker or clearer than other area of the same segment</td><td>Reject</td><td></td></tr>
<tr><td>Misalignment</td><td>Segment fatter or smaller or extra segment</td><td>Reject if > 10% of designed segment width and visible at 30cm distance</td><td></td></tr>
<tr><td>Segment Smearing</td><td>Light up segment smear</td><td>Reject</td><td></td></tr>
<tr><td>Dim segment</td><td>Display shows poor contrast at pre set voltage</td><td>Reject</td><td></td></tr>
</table>

11.2.5 Black Spot, White Spot and Foreign Material (Solid Figure)

Defect Category	Defect Description	Criterion				Drawing Specification
Black Spot, White Spot and Foreign Material	Black Spot, White Spot and Foreign Material	Zone / Dimension	Acceptable No.			 D = (A + B)/2
			A	B	C	
		D ≤ 0.10mm	NC	NC	NC	
		0.10<D ≤ 0.15mm	3	3	NC	
		0.15 < D ≤ 0.25mm	1	2	NC	
		0.25 < D ≤ 0.35mm	1	1	NC	
		D > 0.35 mm	0	0	NC	
		NC: No count D: Mean Diameter of Defect				

*Note: The 1/3 or larger parts of individual dot has to be lighted on.
The solid figure is that the defect has clear-cut outline at the optimum driving condition in both positive and negative, of which size does not change when the contrast changes.

11.2.6 Black Spot, White Spot and Foreign Material (Faded Figure)

Defect Category	Defect Description	Criterion				Drawing Specification
Black Spot, White Spot and Foreign Material	Black Spot, White Spot and Foreign Material	Zone / Dimension	Acceptable No.			 D = (A + B)/2
			A	B	C	
		D ≤ 0.60mm	NC	NC	NC	
		0.60<D ≤ 0.70mm	3		NC	
		0.70 < D ≤ 0.80mm	1		NC	
		D > 0.80 mm	0		NC	
		NC: No count D: Mean Diameter of Defect				

*Note: Faded figure means that the defects has unclear outline at the optimum driving condition in both positive and negative, of which size seems to change when the contrast changes.

11.2.7 Line Shape and Scratches

<table>
<tr><th>Defect Category</th><th>Defect Description</th><th colspan="5">Criterion</th><th>Drawing Specification</th></tr>
<tr><td rowspan="6">Line shape and scratches</td><td rowspan="6">Line shape and scratches</td><td colspan="5"></td><td rowspan="6"></td></tr>
<tr><td colspan="2">Zone /Dimension</td><td colspan="3">Acceptable No.</td></tr>
<tr><td>X</td><td>Y</td><td>A</td><td>B</td><td>C</td></tr>
<tr><td>NC</td><td>≤ 0.03mm</td><td>NC</td><td>NC</td><td>NC</td></tr>
<tr><td>≤ 2 mm</td><td>≤ 0.05mm</td><td>1</td><td>1</td><td>NC</td></tr>
<tr><td>≤ 1 mm</td><td>≤ 0.10mm</td><td>1</td><td>2</td><td>NC</td></tr>
<tr><td>NC</td><td>≥ 0.10mm</td><td colspan="3">Due to (1) round defect</td></tr>
</table>

*Note: Length is X and Width is Y.

REMARK:

i) Total amount of spot defects including round and linear – A total of 5 permissible numbers of defects in Zone A & B including above (12.2.5), (12.2.6), (12.2.7). Regardless of number of defects, the minimum distance between individual defects have to be 5mm or larger.

ii) All the other items of inspection that are not included herein must be determined by the “Limit Standard” sample, which were occasionally set up with the mutual consent of both parties. In every case of the items set up with the Limit Standard, the Limit Standard always takes precedence over the other means of definition.

12.0 Precaution for using LCM.

1. Liquid Crystal Display (LCD)

LCD is made up of glass, organic sealant, organic fluid and polymer based polarizers. The following precautions should be taken when handling.

a) Keep the temperature within the range of use and storage. Excessive temperature and humidity could cause polarization degredation, polarizer peel off or bubble.

b) Do not contact the exposed polarizer with anything harder than HB pencil lead. To clean dust off the display surface, wipe gently with cotton, chamois or other soft material soaked in petroleum benzin.

c) Wipe off saliva or water drops immediately. Contact with water over a long period of time may cause polarizer deformation or colour fading, while an active LCD with water condensation on its surface will cause corrosion of ITO electrodes.

d) Glass can be easily chipped or cracked from rough handling, especially at corners and edges.

e) Do not drive LCD with DC voltage.

2. Liquid Crystal Display Modules.

2.1 Mechanical Considerations

LCM are assembled and adjusted with a high degree of precision. Avoid excessive shocks and do not make any alterations or modification. The following should be noted.

a) Do not tamper in any way with the tabs on the metal frame.

b) Do not modify the PCB by drilling extra holes, changing its outline, moving its component or modifying its pattern.

c) Do not touch the elastomer connector, especially insert a backlight panel (for example, EL)

d) When mounting a LCM make sure that the PCB is not under any stress such as bending or twisting. Elastomer contacts are very delicate and missing pixels could result from slight dislocation of any of the elements.

e) Avoid pressing on the metal bezel, otherwise the elastomer connector could be deformed and lose contact, resulting in missing pixels.

2.2 Static Electricity

LCM contains CMOS LSI's and the same precaution for such devices should apply, namely

a) The operator should be grounded whenever he/she comes into contact with the module. Never touch any of the conductive parts such as the LSI pads, the copper leads on the PCB and the interface terminals with any parts of the human body.

b) The modules should be kept in antistatic bags or other containers to static for storage.

c) Only properly grounded soldering irons should be used.

d) If an electric screwdriver is used, it should be well grounded and shielded from commutator spark.

e) The normal static prevention measures should be observed for work clothes and working benches, the latter conductive (rubber) mat is recommended.

f) Since dry air is inductive to statics, a relative humidity of 50-60% is recommended.

2.3 Soldering

a) Solder only to the I/O terminals.

b) Use only soldering irons with proper grounding and no leakage.

c) Soldering temperature: 280 °C

d) Soldering time: 3 to 4 sec

e) Use eutectic solder with resin flux fill.

f) If flux is used, the LCD surface should be covered to avoid flux spatters. Flux residue should be removed afterwards.

2.4 Operation

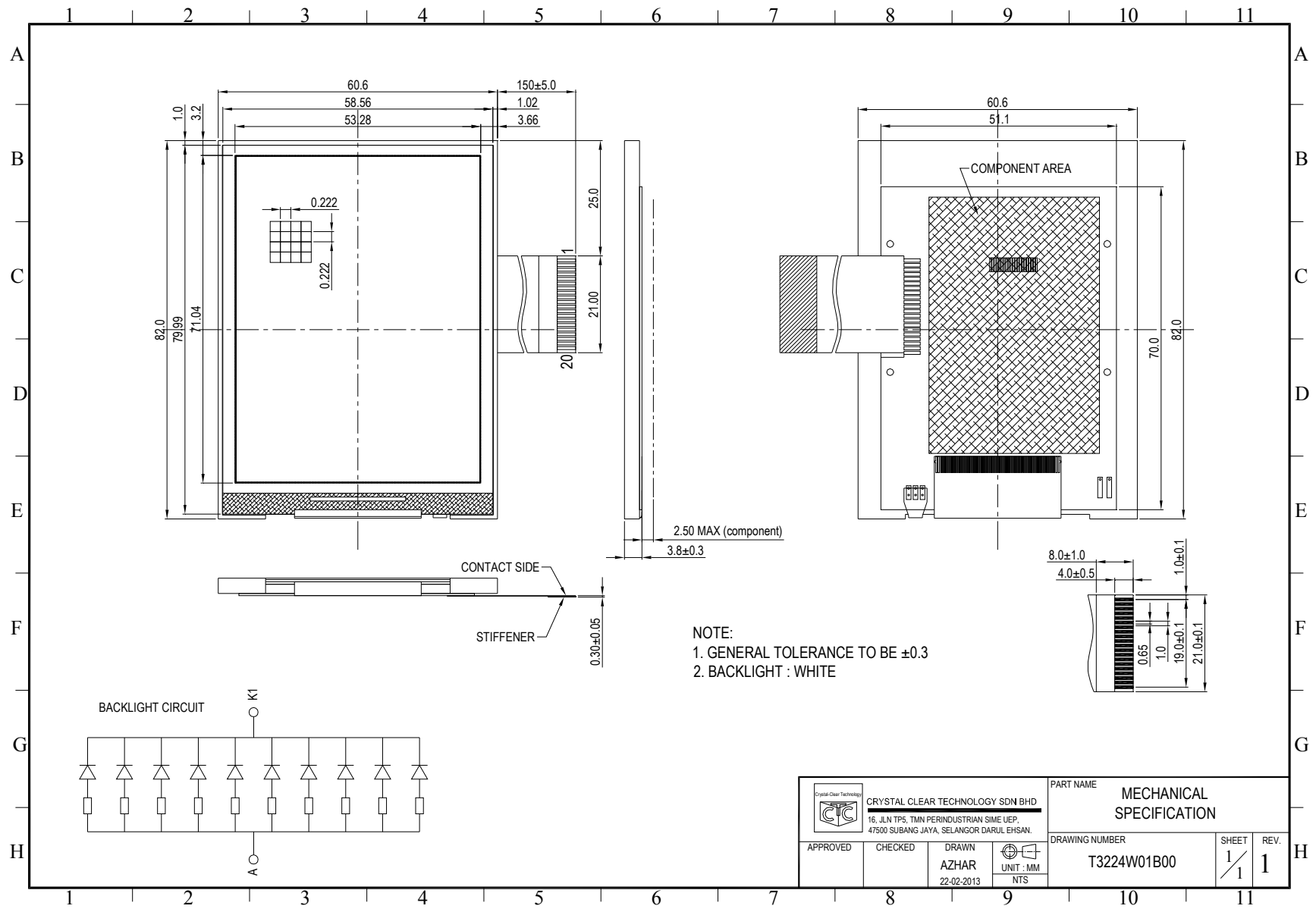
a) The contras can be adjusted by varying the LCD driving voltage V0
b) Driving voltage should be kept within specified range, excess voltage shortens display life.
c) Response time increases with decrease in temperature.
d) Display may turn black or dark blue at temperature above its operational range, this is (however not pressing on the viewing area) may cause the segments to appear “fractured”.
e) Mechanical disturbance during operation (such as pressing on the viewing area) may cause the segments to appear “fractured”.

2.5 Storage

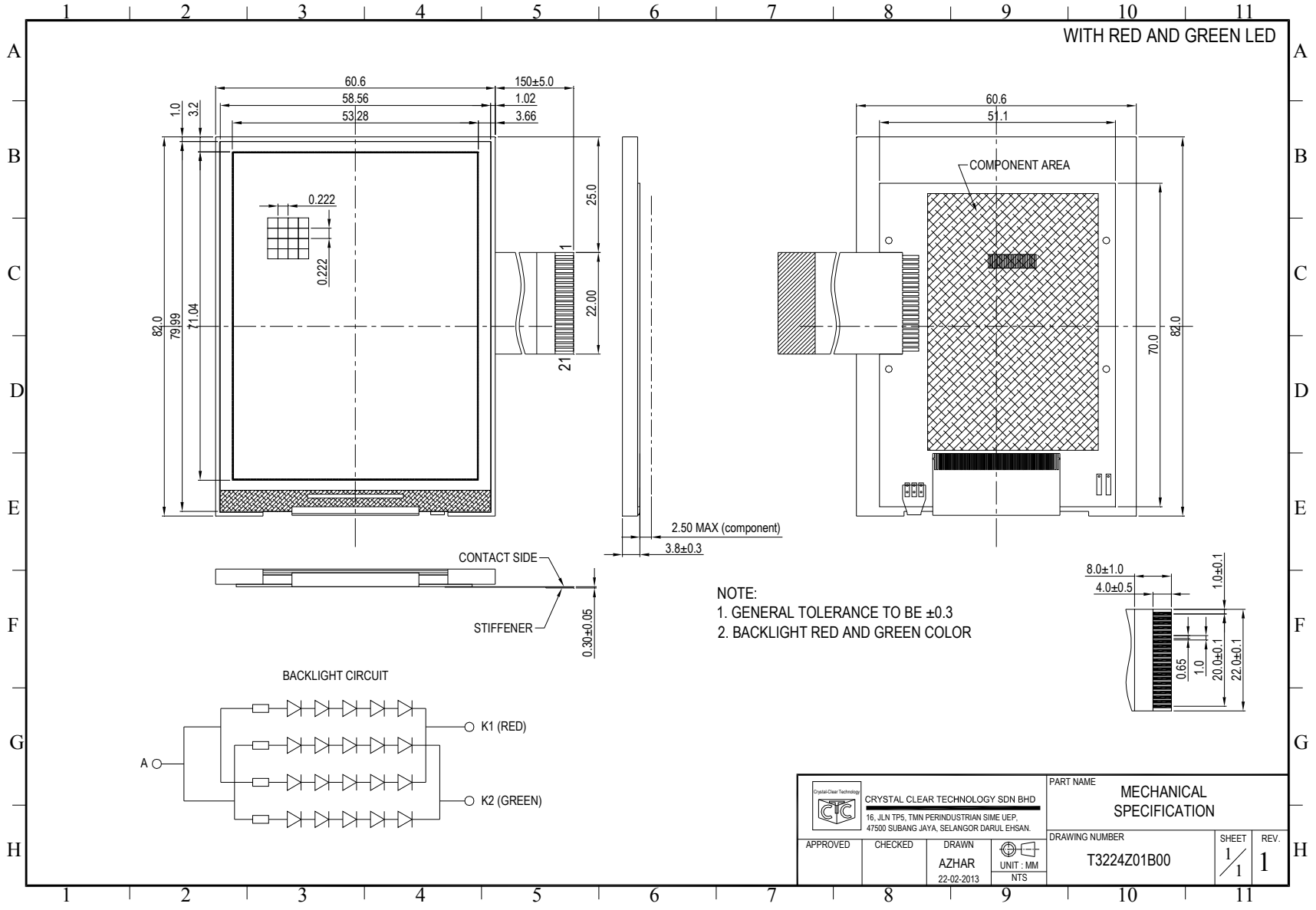
If any fluid leaks out of the damage glass cell, wash off any human part that comes into contact with soap and water. Never swallow the fluid. The toxicity is extremely low but caution should be exercised at all the time.

2.6 Limited Warranty

Unless otherwise agreed between Crystal Clear Technology and customer, Crystal Clear Technology will replace or repair any of its LCD and LCM which is found to be defective electrically and visually when inspected in accordance with Crystal Clear Technology acceptance standards, for a period of one year from date of shipment. Confirmation of such date shall be based on freight documents. The warranty liability of Crystal Clear Technology is limited to repair and/or replacement on the terms set forth above. Crystal Clear Technology will not responsible for any subsequent or consequential events.


60.6
58.56
53.28
150±5.0
1.02
3.66
1.0
3.2
0.222
0.222
25.0
21.00
1
20
82.0
79.99
71.04
2.50 MAX (component)
3.8±0.3
CONTACT SIDE
STIFFENER
0.30±0.05
60.6
51.1
COMPONENT AREA
70.0
82.0
8.0±1.0
4.0±0.5
1.0±0.1
0.65
1.0
19.0±0.1
21.0±0.1
NOTE:
1. GENERAL TOLERANCE TO BE ±0.3
2. BACKLIGHT : WHITE
BACKLIGHT CIRCUIT
K1
A
CRYSTAL CLEAR TECHNOLOGY SDN BHD
16, JLN TP5, TMN PERINDUSTRIAN SIME UEP,
47500 SUBANG JAYA, SELANGOR DARUL EHSAN.
PART NAME
MECHANICAL SPECIFICATION
APPROVED
CHECKED
DRAWN
AZHAR
22-02-2013
UNIT : MM
NTS
DRAWING NUMBER
T3224W01B00
SHEET
1/1
REV.
1

WITH RED AND GREEN LED



NOTE:
1. GENERAL TOLERANCE TO BE ±0.3
2. BACKLIGHT RED AND GREEN COLOR

CRYSTAL CLEAR TECHNOLOGY SDN BHD 16, JLN TP5, TMN PERINDUSTRIAN SIME UEP, 47500 SUBANG JAYA, SELANGOR DARUL EHSAN.				PART NAME	MECHANICAL SPECIFICATION	
APPROVED	CHECKED	DRAWN AZHAR 22-02-2013	UNIT : MM NTS	DRAWING NUMBER	T3224Z01B00	SHEET 1/1 REV. 1

Crystal Clear Technology
16 Jalan TP5—Taman Perindustrian Sime UEP
47600 Subang Jaya—Selangor DE
Malaysia